RECEIVED
CENTRAL FAX CENTER
MAR 0 8 2006

Listing of Claims

This listing of claims replaces all prior versions, and listings, of claims in the application:

Claims 1-7. (Canceled)

8. (Currently Amended) A method of transitioning a processor from one operating mode to a second operating mode, comprising:

flushing a first portion of a cache in a first stage;

disabling the first portion;

flushing a second portion of the cache in a second stage, wherein the processor is available between the first stage and the second stage;

transitioning the processor from the one ~~operating mode~~ state in which code is executed to ~~the~~ a second ~~operating mode~~ state in which code is not executed; and

enabling the disabled portions of the cache.

9. (Previously Presented) The method of claim 8 wherein transitioning the processor from one operating mode to the second operating mode comprises transitioning the processor from one processor mode within the G0 working state to a second processor mode within the G0 working state.

Claims 10-30. (Canceled)

31. (Previously Presented) The method of claim 8, further comprising functionally dividing the cache into the first portion and the second portion prior to flushing the first portion.

32. (Previously Presented) The method of claim 8, wherein disabling the first portion comprises disabling the first portion once the flushing of the first portion is complete.

33. (Previously Presented) ~~The~~ A method ~~of claim 8,~~ ~~further~~ of transitioning a processor from one operating mode to a second operating mode, comprising:

flushing a first portion of a cache in a first stage;

disabling the first portion;

flushing a second portion of the cache in a second stage, wherein the processor is available between the first stage and the second stage;

servicing an interrupt when the processor is available;

transitioning the processor from the one operating mode to the second operating mode; and

enabling the disabled portions of the cache.

34. (Previously Presented) The method of claim 8, further comprising accessing a memory location when the processor is available.

35. (Previously Presented) The method of claim 8, further comprising flushing a third portion of the cache in a third stage, wherein the processor is available between the second stage and the third stage.

36. (Previously Presented) The method of claim 8, wherein the first portion of the cache is larger than the second portion of the cache.

37. (Previously Presented) ~~The~~ A method ~~of claim 8, further~~ of transitioning a processor from one operating mode to a second operating mode, comprising:

flushing a first portion of a cache in a first stage;

disabling the first portion;

flushing a second portion of the cache in a second stage, wherein the processor is available between the first stage and the second stage;

transitioning the processor from the one operating mode to the second operating mode; and

enabling the disabled portions of the cache; and

enabling interrupts after transitioning from the one operating mode to the second operating mode.

38. (Currently Amended) ~~The~~ A method ~~of claim 8, further~~ of transitioning a processor from one operating mode to a second operating mode, comprising:

modifying the cache flush instruction prior to flushing ~~the~~ a first portion of the cache

flushing the first portion of a cache in a first stage;

disabling the first portion;

flushing a second portion of the cache in a second stage, wherein the processor is available between the first stage and the second stage;

transitioning the processor from the one operating mode to the second operating mode; and

enabling the disabled portions of the cache.

39. (Previously Presented) The method of claim 8, wherein flushing the first portion of the cache comprises flushing the first portion of a L1 primary cache.

40. (Currently Amended) The method of claim ~~8~~ 38 wherein transitioning from one operating mode to the second operating mode comprises transitioning a processor from a state in which code is executed to a second state in which code is not executed.

41. (Currently Amended) An article comprising a machine-readable medium storing instructions for transitioning a processor from one operating mode to a second operating mode, the instructions operable to cause operations comprising:

flushing a first portion of a cache in a first stage;

disabling the first portion;

flushing a second portion of the cache in a second stage, wherein the processor is available between the first stage and the second stage;

transitioning the processor from the one ~~operating mode~~ state in which code is executed to ~~the~~ a second ~~operating mode~~ state in which code is not executed; and

enabling the disabled portions of the cache.

42. (Previously Presented) The article of claim 41 wherein transitioning the processor from one operating mode to the second operating mode comprises transitioning the processor from one processor mode within the G0 working state to a second processor mode within the G0 working state.

43. (Previously Presented) The article of claim 41, wherein the operations further comprise functionally dividing the cache into the first portion and the second portion prior to flushing the first portion.

44. (Previously Presented) The article of claim 41, wherein disabling the first portion comprises disabling the first portion once the flushing of the first portion is complete.

45. (Currently Amended) ~~The~~ An article ~~of claim 41, wherein the operations further comprise~~ comprising a machine-readable medium storing instructions for transitioning a processor from one operating mode to a second operating mode, the instructions operable to cause operations comprising: flushing a first portion of a cache in a first stage;

disabling the first portion;

flushing a second portion of the cache in a second stage, wherein the processor is available between the first stage and the second stage;

servicing an interrupt when the processor is available;

transitioning the processor from the one operating mode to the second operating mode; and

enabling the disabled portions of the cache.

46. (Previously Presented) The article of claim 41, wherein the operations further comprise accessing a memory location when the processor is available.

47. (Previously Presented) The article of claim 41, wherein the operations further comprise flushing a third portion of the cache in a third stage, wherein the processor is available between the second stage and the third stage.

48. (Previously Presented) The article of claim 41, wherein the first portion of the cache is larger than the second portion of the cache.

49. (Currently Amended) ~~The~~ An article ~~of claim 41, wherein the operations further comprise~~ comprising a machine-readable medium storing instructions for transitioning a processor from one operating mode to a second operating mode, the instructions operable to cause operations comprising:

flushing a first portion of a cache in a first stage;

disabling the first portion;

flushing a second portion of the cache in a second stage, wherein the processor is available between the first stage and the second stage;

transitioning the processor from the one operating mode to the second operating mode; and

enabling the disabled portions of the cache; and enabling interrupts after transitioning from the one operating mode to the second operating mode.

50. (Currently Amended) ~~The~~ An article ~~of claim 41, wherein the operations further comprise~~ comprising a machine-readable medium storing instructions for transitioning a processor from one operating mode to a second operating mode, the instructions operable to cause operations comprising:

modifying the cache flush instruction prior to flushing ~~the~~ a first portion of the cache;

flushing the first portion of a cache in a first stage;

disabling the first portion;

flushing a second portion of the cache in a second stage, wherein the processor is available between the first stage and the second stage;

transitioning the processor from the one operating mode to the second operating mode; and

enabling the disabled portions of the cache.

51. (Previously Presented) The article of claim 41, wherein flushing the first portion of the cache comprises flushing the first portion of a L1 primary cache.

52. (Currently Amended) The article of claim ~~41~~ 49, wherein transitioning from one operating mode to the second operating mode comprises transitioning a processor from a state in which code is executed to a second state in which code is not executed.

53. (New) The method of claim 8, further comprising servicing an interrupt when the processor is available.

54. (New) The method of claim 8, further comprising enabling interrupts after transitioning from the one operating mode to the second operating mode.

55. (New) The article of claim 41, wherein the operations further comprise servicing an interrupt when the processor is available.

56. (New) The article of claim 41, wherein the operations further comprise enabling interrupts after transitioning from the one operating mode to the second operating mode.